COLLABORATION PROPOSAL

FOR THE IMPLEMENTATION OF FAST ARITHMETIC UNITS

Join us as we take part in the revolution of microprocessors, unlocking untapped mathematical potential that will redefine standards of computing performance and data privacy across multiple sectors including smart cities and grids, Machine Learning such as in specific cases of AI and Neural Network training utilizing sensitive data, Digital Signal Processing and cryptography, among others. A Compute-In-Memory architecture is proposed for the next generation of faster and more efficient processors, as well as new mathematical encryption schemes to set new standards of privacy, reliability and efficiency in AI training.

My mathematical research provides an optimal representation of mathematical objects and structures [1,2,3] with direct applications in computer science [4,5,6], and the mathematical foundations of computer science. Leveraging this new mathematical description, we seek to create value by offering efficient technological solutions to a range of industries. Among these solutions is an Arithmetic Logic Unit (ALU) design, with unique capabilities and characteristics, that solves the existing Von-Neumann Bottleneck with a simple and scalable Compute-In-Memory architecture [5,6], that has been patented in the relevant countries.

The present proposal focuses on this processor architecture. Through strategic partnerships and collaborations, we are poised to drive innovation and create a competitive edge in the rapidly evolving technological landscape, by implementing time and energy efficient processing with a low-cost scalable ALU design. A separate proposal will discuss software-level implementations of a secure and efficient Homomorphic Encryption scheme.

REPORT AUTHOR

Juan P. Ramírez

ALLIANCES
Partners / Clients

We look to work with experts, institutions and businesses

DEVELOPMENT

By working with our clients, we are able to provide custom designed and tailor-fitted critical subunits for digital and analog devices.

Collaborations

Applications and Integration

TEAM

Research
Sr. Engineers

Math - Physics - CS

INDUSTRY

We are positioned to be a driving froce that will impact almost any sector of science and technology.

Revision of mathematical foundations with efficient operations and other applications.

LEADERSHIP

RESEARCH

Through strategic partnerships and collaborations, we will create a competitive edge.

Middle and Final Customer Satisfaction.

INNOVATION

VALUE

PRODUCTS AND SERVICES

First we focus on a new generation of simple yet powerful processors of unmatched capabilites.

A proposal of new mathematical methods yields results in applied physics, numerical methods, cryptography, data mining, high-performance computing among others.

Globally competitive patents for digital and analog systems.

Mathematically optimized architectures for data science, cryptography, analog and digital devices.

Effective Campaigns

MARKETING AND CUSTOMER EXPERIENCE

THEORETICAL FRAMEWORK

Through a fundamental solution to the problem of numerical representations and their computational complexity, we seek to transform the processor industry. This initiative is based on a major revision of mathematical foundations that allows fast and low-powered calculation of mathematical operations at a hardware and software level. The mathematical framework is provided in [1,2,3], along with other supporting papers cited in the bibliography, at the end of this proposal.

Mathematics is the invisible framework supporting scientific progress and technological innovation. Not only does it advance our understanding of abstract concepts, but it also provides practical solutions to real-world challenges because it is the universal language behind all sciences. The coding language that computers understand is built on mathematics. Consequently, by refining the underlying principles of mathematics, we essentially upgrade the 'language' that enables our technology to communicate and perform tasks more efficiently.

In a world pushing the boundaries of innovation, we are reaching the limits of current technological frameworks. Using a novel conceptualization of the foundations of mathematics with immediate applications in a number of key technologies facilitating seamless data representation and computational operations, from high-level software languages down to the System-on-Chip hardware level, we seek to introduce efficiency in ways previously unexplored.

The single most important subunit determining performance, for almost any processor is the ALU (Arithmetic Logic Unit) which can be responsible for 20-50% of all operations executed in an average CPU and can reach more than 80% of operations executed in a GPU [9]. The ALU is even more important, for area-specific integrated circuits (ASICs) used for AI training, data centers, aviation [10], automobiles, communications, geolocation, crypto-mining [11], energy sector, advanced CGI applications, Digital Signal Processing among others. More reference material on ALUs and their functionality, architecture, and specifications are found in [12-17].

In [1,2,3], we propose new foundations of mathematics with applications essential to information technologies and computer sciences including a Simple and Linear Fast Adder (SLFA) with optimized efficiency, complexity, dimensions, and materials costs [5]. A general modified version of the SLFA is compatible with proposed fast-multiplication and fast-derivative (FDA) algorithms, and vector/matrix operations [6].

The FAU (Fast Arithmetic Unit) is a new type of ALU of its own kind with unparalleled performance and efficiency in computing everything from addition of scalars to matrix multiplication (essential for Machine Learning and AI and neural network training, CGI, Digital Signal Processing, and other operation intensive applications), in one simple and scalable circuit.

Problem:
Von-Neumann Architecture of a CPU is characterized for separating memory and the arithmetic logic circuitry (the ALU is where all logical and mathematical operations take place) and connecting them via a bus. This creates a bottle neck in computational throughput because back-and-forth data migration between memory and the ALU is very expensive and generates huge time delays. The need for new architectures and fundamental changes to the approach in designing classic computational schemes has become increasingly apparent.

Solution:

In-Memory Computing is a concept solution proposed decades ago, but still has fundamental challenges to be overcome before it can be fully implemented. The theoretical framework allows for the implementation of a simple circuit, here referred to as Fast Arithmetic Unit (FAU), solving major issues for In-Memory Computing [18] and it is capable of executing low-powered In-Situ ALU operations faster and cheaper, improving overall processor efficiency, in an area smaller than the area occupied by a traditional fast-adder. This unit is also capable of calculating a fast derivative approximation (FDA), and fast vector multiplication, making the FAU of central importance for AI hardware and other TPU (Tensor Processing Unit) applications that require processing vector/matrix operations faster and cheaper.

Why FAU?

Replacement of traditional ALUs for FAU technology, in general and specific use processors, will:

- Significantly Improve Performance
- Provide Unparalleled Capabilities and Characteristics
- Optimize Energy Efficiency
- Facilitate Compatibility with Many Industries
- Advance In-Memory Computing
- Allow One-size fits-all Circuit for all ALU Operations

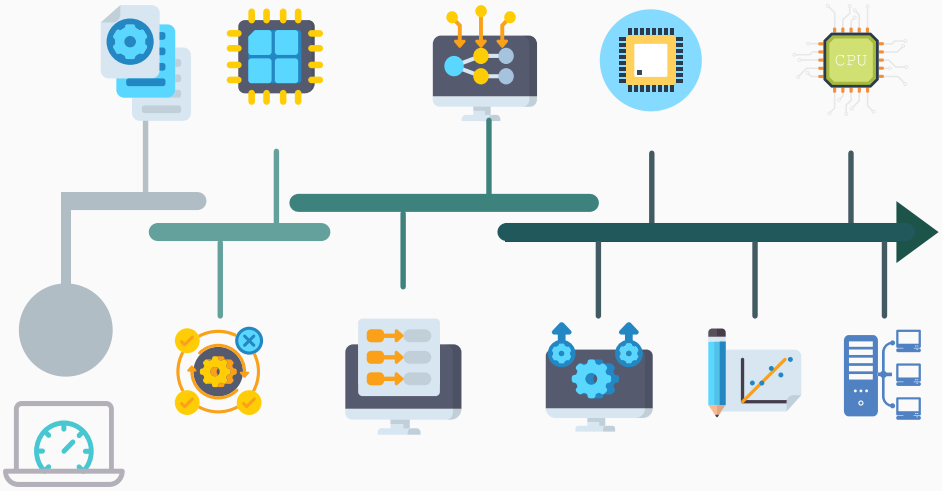
What's Next?

1. Develop FAU prototypes that improve on efficiency and performance and integrate the FAU architecture to existing standards.
2. Collaborate with ASIC designing teams and adapt our technology to their needs, in order to secure contracts and financing of operations.
3. Facilitating the replacement of traditional ALUs with FAU, in ASICs.
4. Consolidating research and developing capabilities for integrating FAU to high-performance VLSI architectures.

PROGRESS STAGES

0. Validation
1. First R+D Stage: Identifying Immediate Industries, Patents, Prototypes
2. Integration to ASIC Design Standards
3. Integration to ASIC Production Standards
4. Second R+D Stage: Consolidating Research
5. Digital Operations and Output Management (GPU and CPU)

Progress:
We have commenced progress on stages 0 and 1 with a successful WIPO patent application [5], a published paper [6] and numerous conferences that can be consulted on page 27 under "Participations".



STAGE (0): VALIDATION

Summary

In an area smaller than other fast adders, the FAU is able to execute fast addition and multiplication, and other higher order operations (operations defined in terms of addition and multiplication, and operations defined in terms of those, etc.) such as subtraction and division. Furthermore, the FAU can fast approximate a numerical derivative, giving the FAU unmatched capabilities, functionality and efficiency, all in a simple design with minimum surface area.

The two main activities for this stage are 1) Publishing and comparing results with existing ALU architectures [19,20] and 2) Simulating the proposed FAU architecture.

Publishing

The simulation results are compared and evaluated against results from existing architectures.

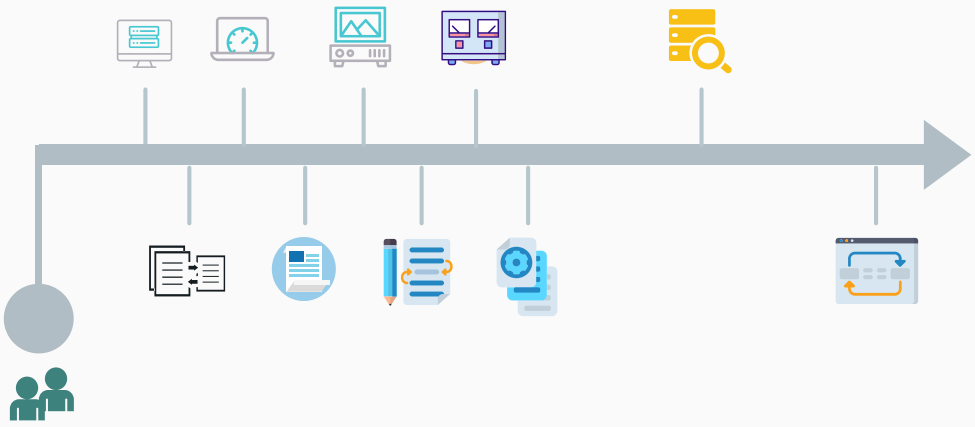
The conclusions are to be shared in international editorials and will help determine resources, objectives and strategies for the next stages.

Simulating

During this stage, simulations on the implementation of the FAU are carried out using tools such as VHDL, Verilog and FPGA.

OBJECTIVES FOR STAGE (0)

- Build a Core R&D Team
- Simulate Fast Arithmetic Unit (FAU) Architecture
- Publish Results
- Conclusions and Planning for Next Stages



THE TEAM FOR STAGE (0)

A team of specialists in computer science, physics and mathematics will lay the groundwork for specialized, state-of-the-art, arithmetic units to be implemented in high-performance processors.

The team will be able to propose and expand new lines of research for Computing-In-Memory architectures, control units for ASICs, material optimization, operation optimization, non-classic architectures such as photonic computing schemes, cryptography, AI and Neural Network training HW.

Hardware

A team of C.S. Engs. with experience in ALU architecture to determine best materials, configurations, instructions, layouts, i/o to CU and other variables through FPGA simulations.

Software

The initial simulations need to be carried out in collaboration with a team of SW Engs. using FPGA and HW description languages (HDL) such as Verilog and VHDL.

Mathematics

A mathematics team covers the basic areas of number theory, mathematical analysis, matrix analysis, computational geometry, AI, Probability Theory, Finite Mathematics and Combinatorics, Algebra and Logics, will help to choose the best research topics for later stages.

Physics

An important part of the initial research is dependent of a physics team to complement the research with the Electromagnetic Theory, Signal Processing, Material Science for Semiconductors, among others topics.

STAGE (1): IDENTIFYING IMMEDIATE INDUSTRIES, PATENTS, PROTOTYPES

Summary

ALUs are circuits implemented on different scales, for different applications, with different materials, configurations, layouts and topologies, distinct kinds of memory elements, etc. This makes the FAU a disruptive technology applicable to a wide variety of industries.

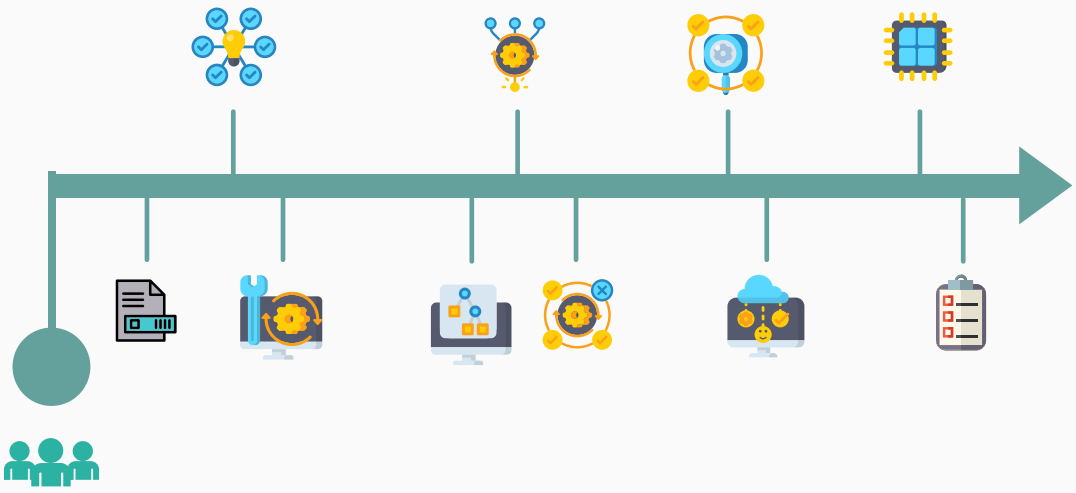
This stage comes after a careful evaluation of the main applications. In this stage we will look for the best industries for immediate implementation by identifying the simplest processors that can benefit most from the FAU in a fast and seamless manner.

Immediate implementation candidates are selected by taking into account technical analysis, company objectives, and market demand. Then, we secure the respective patents and designs that are prioritized for immediate implementation.

The main objectives of this stage are to design, evaluate and improve prototypes for the selected industries.

OBJECTIVES FOR STAGE (1)

- Consolidate and Expand the Team
- Identify Critical Patents from the Theoretical Framework
- Reduce Candidate Implementations Prioritizing Quickness and Simplicity
- Identifying Industries and Clients for Immediate Implementation
- Developing and Evaluating Prototypes



THE TEAM FOR STAGE (1)

Meeting the goals set out for this stage will require the expansion of our Architecture and Hardware team to include a technical base in design and prototyping of ASICs, centered on the In-Situ computing scheme of the SLFA which is pending PCT patent approval).

The SW team will need expertise in Low-Level Languages (LLL) for conducting research on the appropriate LLL that will help to integrate the FAU into existing assembly.

ALU Architecture

The HW team will need to include specialists on ALUs and Registers/memory elements.

Integrated Circuits

Operations in the HW area will require a knowledge base in designing and prototyping stages of ICs.

Software

For Assembly Language we will require the participation of SW specialists on LLL, Computational Logic and Information Theory.

STAGE (2): INTEGRATION TO ASIC DESIGN STANDARDS

Summary

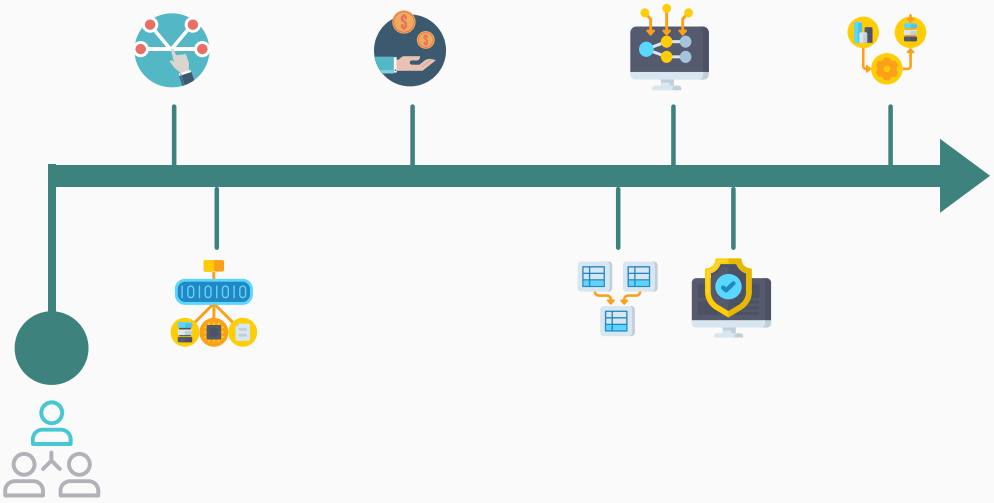
Once the immediate implementation industries are recognized and prioritized by simplicity and speed of integration, along with their preliminary technical aspects, we proceed to integrate the FAU to current design standards.

We seek collaboration with participants in the processor industry to replace existing ALUs with FAU architecture. The first applications will be in medium scale integration circuits with simple Control Unit. These can include commercial use ASICs used in smart appliances and electronics, GPS, automobiles, energy sector, communications, mathematical research, data mining, etc.

During this stage we seek to collaborate with ASIC manufacturers from different commercial and scientific applications, in order to secure continuity of operations. Our potential clients and partners for this stage are mostly in S. Korea, Singapore, India, Russia, China, Japan, Germany, France, UK and US. Strategic collaborations could include names such as Hana Micron, Samsung Electronics; Singapore Semiconductor Industries Association; Tata Elxsi, Vedanta; Sitronics, Mikron Group; SMIC, Pythium, Foxconn, HiSilicon; Japan Advanced Semiconductor Manufacturing, Fujitsu; Infineon Technologies AG, Siemens; STMicroelectronics; ARM; Texas Instruments, Qualcomm, Amkor, Xilinx, Altera, ONSEMI, Analog Devices Inc., Intel, etc.

OBJECTIVES FOR STAGE (2)

- Find Sr. Engs. and Team Leadership
- Establish Collaboration with Industry Clients
- Secure Contracts for Integrating FAU in ASICs
- Integrate Our Designs to Client Standards
- Simplify the Replacement of Traditional ALUs for FAU



THE TEAM OF STAGE (2)

The incorporation of FAU into ASICs requires collaboration with clients. In this stage new variables are considered such as i/o to the Control Unit for parametrizing "Clock", instruction sets, connections, etc.

Control Unit (CU)

We must work with clients' teams in charge of CU architecture for ASICs.

Registers

In particular, we must work with teams in charge of memory registers.

Software

Collaboration with our clients' LLL teams responsible for machine and assembly language.

Hardware

Other HW aspects outside the CU such as connections, buses, i/o control, etc.

STAGE (3): INTEGRATION TO ASIC PRODUCTION STANDARDS

Summary

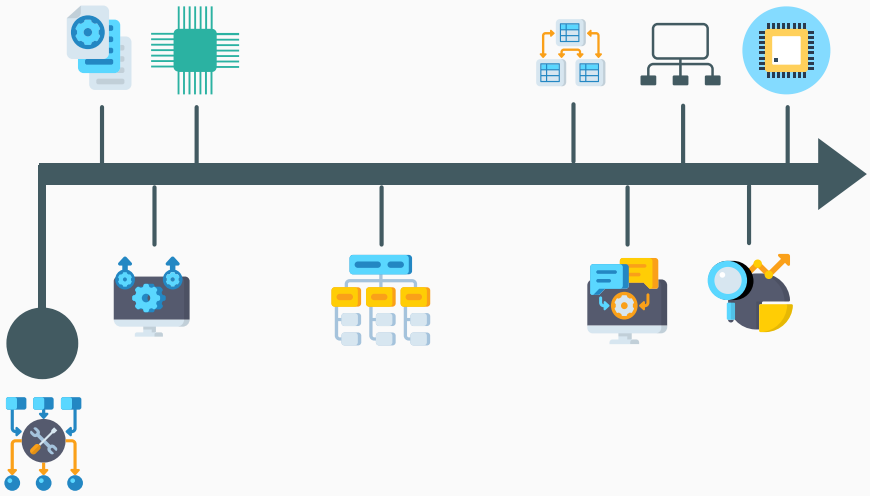
In the previous stage, we work together with our clients' teams during the designing stages of their ASICs, substituting the ALU for an FAU tailored to their specific needs.

The objectives of this new stage are divided in two. First, that our clients conclude successful production of processors with FAU technology. We maintain collaboration during their transition to production, as they may require it. Cooperation with them will be essential during testing, troubleshooting, quality monitoring, etc.

Secondly, this stage will serve to develop our internal capabilities. Among them, the implementation of the FAU to a larger class of ASIC architectures.

OBJECTIVES OF STAGE (3)

- Helping Our Clients Conclude Successful Production of ASICs with FAU Technology
- R+D for implementing FAU in Additional Platforms
- Achieving Universality of FAU in ASICs

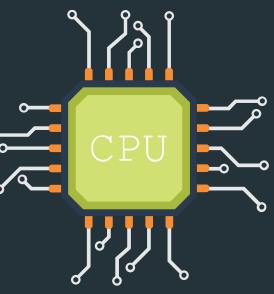


STAGE (4): CONSOLIDATING RESEARCH

Summary

This stage will set practical and theoretical objectives. In practical terms, we will develop necessary capabilities for the designing stages leading to the integration of the FAU to VLSI circuits. We wish to implement FAU into more profitable architectures such as general-purpose RISC and other high-performance architectures with broad functionality. The groundwork for these long-term goals begins in this stage.

During this stage, we also drive R+D into other areas and applications proposed in the theoretical framework. These include topics in Numerical Methods, Matrix Analysis, Cryptography, Applied Physics, Finite Mathematics, Data Science, an analog version of the SLFA based on coupled waves [21] and more.



STAGE (5): DIGITAL OPERATIONS AND OUTPUT MANAGEMENT

Summary

The previous stage has the purpose of developing basic design capabilities for integration of FAU into VLSI architecture. This stage is for research and development of a production model for high-performance general and specific purpose architectures, to address a growing demand on integrating computational efficiency, in all of its stages and levels from hardware to LLL.

MARKET SHARE PROJECTIONS

The proposed FAU technology can significantly improve processor efficiency, performance and throughput, and can be applied in a wide range of industries including Machine Learning and AI, data centers, consumer electronics, CGI, cryptography [6] and many others.

Let us take AI, as an example. In a study, by MarketsandMarkets, this industry is estimated to grow from USD $28 billion in 2020 to USD $126 billion by 2025, representing a compound annual growth rate (CAGR) of 34.5%. It is estimated that by 2030, the total market value will be USD $807 billion.

According to another report, by Precedence Research, the global AI microprocessors market is projected to grow from USD $16.86 billion in 2022 to USD $227.48 billion in 2032, representing a CAGR of 29.72%. Participation in only a fraction of the AI microprocessors market represents great revenue opportunities.

The long-term trend of microprocessors market share in the AI industry will be between 20% and 30% of total industry capitalization. A participation of just 1% with 20% profit margin means more than USD $80 million in potential net income, for the year 2026 alone.

In 2021 the total capitalization value of automobile CPUs was estimated at USD $53 billion. And these are just a few examples. FAU technology has the potential for competitive innovation in many sectors of science and technology.

LET'S PARTNER

Applications of the proposed FAU can be adapted and scaled to other industries and applications from those mentioned above, creating more revenue sources in the long-term as well. By developing a strategic plan for commercialization and growth, we can achieve a lasting projection of high ROI for our investors.

To secure the necessary resources for research and development, we seek strategic collaborations and partnership with academic, and research experts, as well as industry leading institutions. Together, we can advance this unique focus into the world of cryptography, computational throughput and other critical technologies, acquiring a strategic advantage in the changing technological landscape.

As we stand at the forefront of current innovations, we invite you to push the boundaries of mathematical theory with us. Tangible solutions to today's social and technical challenges, of increasing complexity and breadth, are possible through a long-term horizontal and vertical integration of mathematically optimal computational standards across all devices and systems. While our work may appear theoretical, its impact is far-reaching in the technology-driven world we live in and seeks to lay foundation for more efficient and secure computing at every level.

Join us in this exciting journey. Thank you!

Juan P. Ramírez
Project Leader

STRATEGIES

Leadership

- New approach to state-of-the-art designs for critical subunits in special and general-purpose architectures.
- Exploring new research areas with applications to high-performance computing.

Innovation

- Driving the development of optimized subunits.
- Collaboration in R+D, with partners of relevant industries and institutions.
- Innovate industrial and academic research by reformulating applicable mathematical foundations.

Services and Products

- Integrating mathematically optimized designs into digital and analog systems.
- High-value utility patents with global competitivity in digital and analog devices.

Marketing and Customer Experience

- Web Development.
- Effective Campaigns.
- Middle and final customer satisfaction.

EARLY TACTICS

- [x] Generate world class Research in Applied Mathematics and Computer Sciences.
- [x] Participation in key international conferences and symposiums.
- [ ] Validate the new ALU architecture and compare the results to existing designs.
- [ ] Collaboration and strategic alliances with clients and partners.
- [ ] Early marketing strategies for connecting to general and targeted public.

MISSION

Maintaining our clients at the forefront of fundamental processes in digital technologies through global high-value patents and world-class R+D.

As well as the responsible integration of technological solutions and the exploration of state-of-the-art applications that enrich experiences for general public, scientists and artists.

VISION

Modern anthropological sciences and technological development from AI to Social Organization, are product of interactions between humanities and natural sciences.

The greatest challenges that science must solve are related to human realities and are growing in complexity and breadth.

Recognizing that the nature of our most critical problems is socio-technical, a better comprehension of solutions and implementations will be possible.

BIBLIOGRAPHY

[1] Ramírez, Juan Pablo. 2023. "Canonical Set Theory with Application from Parallel Matrix Operations and Data Structures to Homomorphic Encryption".
Exclusively on Author's personal page: www.binaryprojx.com

[2] Ramírez, Juan Pablo. 2019. "A New Set Theory for Analysis" *Axioms* 8, no. 1: 31. https://doi.org/10.3390/axioms8010031.

[3] Ramirez, J. 2015. Systems and Categories. arXiv:1509.03649v5 [math.CT]

[4] Ramirez, J. 2024. "Programming Random Change of Variables for Homomorphic Encryption."
White Paper Exclusively on Author's personal homepage: www.binaryprojx.com

[5] J. P. Ramírez, "Simple and Linear Fast Adder of Multiple Inputs and Its Implementation in a Compute-In-Memory Architecture," 2024 International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA), Victoria, Seychelles, 2024, pp. 1-11,
doi: 10.1109/ACDSA59508.2024.10467957.

[6] Ramirez, J. "SIMPLE AND LINEAR FAST ADDER," WIPO, Patentscope.
Publication Number: WO/2023/220537.
Publication Date: 16/11/2023.
Applicant's and Inventor's name: Juan Pablo Ramirez

[7] Ronald L. Rivest, Len Adleman, and Michael L. Detouzos. On data banks and privacy homomorphisms. In Foundations of Secure Computation, pages 165–179. Academic Press, 1978. Available at https://people.csail.mit.edu/rivest/pubs.html#RAD78.

[8] C. Gentry, (2009). "A Fully Homomorphic Encryption Scheme," Doctoral Dissertation, Symposium on the Theory of Computing, NY, New York, USA, 2009.

[9] Hennessy, J.L. and Patterson, D.A. (1990) Computer Architecture: A Quantitative Approach. Morgan Kaufmann, Waltham.

[10] Andrew Reilly. Multi-Core Processors are the Key to Unlocking Aviation's Future. AeroSpaceTechReview.com (Nov. 10, 2020).

[11] Yiqiu Sun, Haichao Yang, et. al. ASIC Design for Bitcoin Mining. University of Michigan.

[12] Miguel Albert Orenga, Gerard Enrique Manonellas. Estructura de Computadores, Módulo 7: La Arquitectura CISCA. Universitat Oberta Catalunya.

[13] M.S. Schmalz. Organization of Computer Systems, Section 3: Computer Arithmetic. University of Florida.

[14] Abrar, M., Elahi, H., Ahmad, B.A. et al. An area-optimized N-bit multiplication technique using N/2-bit multiplication algorithm. SN Appl. Sci. 1, 1348 (2019).
https://doi.org/10.1007/s42452-019-1367-6

BIBLIOGRAPHY

[15] Niall Emmart and Charles C. Weems. High Precision Integer Multiplication with a GPU Using Strassen's Algorithm with Multiple FFT Sizes. Parallel Processing Letters, Vol.21, No. 03, pp. 359-375 (2011). https://doi.org/10.1142/S0129626411000266

[16] Arithmetic Logic Units (ALU) Information: Specs.
Globalspec.com

[17] Muhammad Ikmal Mohd Taib, Muhammad Najmi Zikry Nazri, et. al (2020). Design of Multiplication and Division Operation for 16 Bit Arithmetic Logic Unit (ALU). JOURNAL OF ELECTRONIC VOLTAGE AND APPLICATION VOL. 1 NO. 2 (2020) 46-54.
DOI: https://doi.org/10.30880/jeva.2020.01.02.006

[18] Chenyu Wang, Ge Shi, Fei Qiao, Rubin Lin, Shien Wu and Zenan Hu. Research Progress in Architecture and Application of RRAM with Computing-In-Memory. Nanoscale Adv., 2023, 5, 1559-1573.

[19] R. Uma, Vidya Vijayan, et. al. Area, Delay, and Power Comparison of Adder Topologies. International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.

[20] Singh, Kumar and Singh. Performance Analysis of Fast Adders Using VHDL. 2009 International Conference on Advances in Recent Technologies in Communication and Computing.

[21] Xie, Jingya, Niu, Xinxiang, Hu, Xiaoyong, Wang, Feifan, Chai, Zhen, Yang, Hong and Gong, Qihuang. "Ultracompact all-optical full-adder and half-adder based on nonlinear plasmonic nanocavities" Nanophotonics 6, no. 5 (2017): 1161-1173. https://doi.org/10.1515/nanoph-2017-0035

JUAN PABLO RAMÍREZ

PHONE NUMBERS:

+1 (708) 945 - 4477

EMAIL AND PERSONAL PAGE:

jramirez@binaryprojx.com
www.binaryprojx.com

ADDRESS:

Guadalajara, Jalisco, México

EDUCATION

UNIVERSIDAD DE GUADALAJARA

2008 - 2011, Guadalajara, México

1. Teaching experience
2. Served in panels for designing new academic programs in Natural Sciences and Engineering
3. Speaker at International Conferences and Symposiums
4. Participation and Leadership in academic and industrial research and application programs
5. Developing and solving mathematical models for Theoretical Physics, with Dr. Georgi Pogosyan of the International Center for Advanced Studies and the Joint Institute for Nuclear Research
6. Applied Mathematics with Dr. Alexander Yakhnov, from the Dept. of Mathematics
7. Project managing and Director of events such as workshops and "Art and Science Week"
8. Experience in software development and managing high-level to low-level language projects

UNIVERSIDAD DE GUANAJUATO Y CENTRO DE INVESTIGACIÓN EN MATEMÁTICAS (CIMAT)

2011 - 2013, Cd. Guanajuato, México

1. Research presented at area-specific conferences and seminars
2. Activities divulging mathematical sciences

LANGUAGES

English
Spanish
C++
Python
MySql
Java
JavaScript

RESEARCH AREAS

Mathematics

Physics

Computer Sciences

RESEARCH TOPICS

- General Theory of Systems
- Axiomatic Basis and Mathematical Foundations
- Numeric Solutions
- Recursivity
- ALU Architecture
- Computability and Complexity
- Category Theory
- Logical Systems
- Formal Systems and Languages
- Mathematical Analysis
- Cryptography and Homomorphic Encryption
- among other related topics.

PARTICIPATIONS

- "Recursive Solutions for Constant Coefficient Differential Equations". Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2010.
- "Axiomatic Basis for Probability". Second School on Logic and Sets, UNAM campus Morelia, 2013.
- "General Theory of Systems and Algebraic Structures". Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2017.
- "A Natural Construction of Real Numbers". Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2017.
- Workshop on "Mathematics and Paint". Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2018.
- "Topologies of N in the Construction of R". Physical-Mathematical Sciences Week, Universidad de Guadalajara, 2018.
- Organization and Direction of "Art and Sciences Week", including workshops, conferences, roundtables and creation of Smart Mural (Universidad de Guadalajara, 2018, 2022, 2024).
- Workshop on "Higher Order Derivatives for Solving Partial Fractions and their Applications". XIII Encuentro de Especialistas del Norte de Jalisco y Sur de Zacatecas, 2018.
- "The Nature of Numbers". Logic and Foundations Special Session, 52 Mexican Congress of Mathematics, Monterrey, Nuevo León, 2019.
- "The Nature of Numbers". Universidad de Guanajuato/CIMAT, 2019.
- Chicago Quantum Summit. University of Chicago, 2020.
- Smart Mural. Inauguration of 55 Mexican Congress of Mathematics, 2022.
- "Canonical Block Form for Finite Groups". Algebra Special Session, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022.
- "Simple and Linear Fast Adder based on a Simple Representation of Natural and Real Numbers". Computer Science Special Session, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022.
- "Simple Representation of Natural and Real Numbers". Logic and Foundations Special Sessions, 55 Mexican Congress of Mathematics, Guadalajara, Jalisco, 2022.
- "A Pseudo Measure on the Space of Finite Functions and Permutations". Algebra Special Sessions, 56 Mexican Congress of Mathematics, San Luis Potosí, 2023.
- "An Algorithm for Fast Multiplication and Addition of Multiple Inputs and It's Implementation for In-Memory-Computing". Computer Science Special Sessions, 56 Mexican Congress of Mathematics, San Luis Potosí, 2023.
- "Simple and Linear Fast Adder of Multiple Inputs and It's Implementation for a Compute-In-Memory Architecture". International Conference on Artificial Intelligence, Computer, Data Sciences and Applications, 1-2 February 2024, Victoria-Seychelles.
- "Programming Random Change of Variables for Homomorphic Encryption". Modern Methods, Means and Technologies of Information Protection (timed to coincide with the 90th anniversary of its founder, Professor Oleg Borisovich Makarevich, on September 11-15th, Taganrog, Russia.

PUBLICATIONS

- Ramirez, J. 2024. "Programming Random Change of Variables for Homomorphic Encryption". Report on my participation in "Modern Methods, Means and Technologies of Information Protection" 2024 international conference soon available.
- Ramirez, J. 2024. "Programming Random Change of Variables for Homomorphic Encryption". Full White Paper Exclusively on Author's personal page: www.binaryprojx.com
- J. P. Ramírez, "Simple and Linear Fast Adder of Multiple Inputs and Its Implementation in a Compute-In-Memory Architecture," 2024 International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA), Victoria, Seychelles, 2024, pp. 1-11, doi: 10.1109/ACDSA59508.2024.10467957.
- Ramirez, J. "SIMPLE AND LINEAR FAST ADDER," WIPO, Patentscope. Publication Number: WO/2023/220537. Publication Date: 16/11/2023. Applicant's and Inventor's name: Juan Pablo Ramirez
- Ramirez, J. 2023. "Canonical Set Theory with Applications from Matrix Operations and Data Structures to Homomorphic Encryption" Monograph Exclusively on Author's personal home page: www.binaryprojx.com
- J. P. Ramírez. "A New Set Theory for Analysis," Axioms. 2019. 8, no. 1: 31. https://doi.org/10.3390/axioms8010031. Cited by Lovyagin (2021) on the topic of Finite Arithmetic and Non-Standard Analysis for Hyperrationals with Applications to AI.
- Ramírez, J., Londoño W., et. al. "Closed Solution for Partial Fractions" Boletín Redipe, ISSN-e 2256-1536, Vol. 7, Nº. 11, 2018 (Special issue dedicated to: Pedagogical value of the media), págs. 172-178
- Ramirez, J. 2015. Systems and Categories. arXiv:1509.03649v5 [math.CT]

CURRENT PROJECTS

Currently, I am seeking to develop some critical applications, of the mathematical framework I propose, in computer sciences at a software and hardware level ranging from significant optimizations in the representations of numbers and operations, to the algorithms that process and share confidential data.

I am founder of a Research and Development startup, "OPERACIONES DIGITALES Y PROCESAMIENTO INTEGRAL DE DATOS ENCRIPTADOS, SAS" incorporated in Mexico, that studies and integrates mathematical efficiency from a new standpoint that is proving to yield numerous advantages across applications in natural sciences, mathematics and computer sciences.

My current main goals are to establish collaboration and partnering for continuing development on industry level applications, which include a patent for a Simple and Linear Fast Adder that has a scalable design with constant topological complexity and linear growth with respect to the number of input bits. Another direct application of my research includes an encryption scheme that allows encrypted data to be processed, without decrypting it first, which has numerous applications including AI training with sensitive data.